# **REPRODUCING SPECTRE ATTACK WITH GEM5**

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**Consequence**: Micro-architectural security is **hard** 

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**Transient Instruction** 

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⇒ Affects the processor **micro-architectural state** – leaving its architectural state as prior the execution

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### **Transient Instruction**

⇒ Affects the processor **micro-architectural state** – leaving its architectural state as prior the execution

### Spectre

⇒ Execute malicious transient instructions exploiting the **branch predictor** 

## SIMULATION CAN BREAK THIS BLACK BOX

**How**: Allowing the user to view the micro-architecture's behavior





## Cycle-accurate simulator

6

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⇒ Simulate very precisely **hardware** entirely **in software** 

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⇒ Instantiate and parameterize **Python objects** 

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⇒ Simulate very precisely hardware entirely in software
Build a system

⇒ Instantiate and parameterize **Python objects** 

### Run a system

⇒ Launch the Python script, then **view and inspect** the running system!

## **OBSERVING SPECTRE WITH KONATA**

### **SUCCESS SCENARIO**

### Cycles (Time)

12769: s182700 (t0: r3392): 0x0041b430: b.ne 0x41b500					
12770: s182701 (t0: r3393): 0x0041b500: subs x2, #16					
12771: s182702 (t0: r3394): 0x0041b504: b.cs 0x41b528					
12772: s182703 (t0: r3349): 0x0040095c: ret	F DC Rn 1 IS Cm 1				
12773; s182704 (to: r3350); 0x00400054; dsh	F Dc Rn 1 Ds 1 2	2 3 4 Is Cm 1			
12774: :: ldr x1, [sp, #	#28] F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Is Cm 1 2 3	4 5 6 7 8 9 10 11 1	12 13 14 15 16 17 18 19 20 21 22 23
12775: Attacked :: ldr x0, [sp, #	#40] F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Is Cm 1 2 3	4 5 6 7 8 9 10 11 1	12 13 14 15 16 17 18 19 20 21 22 23
12776:: scvtf f0, f1	F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Ds 1 2 3 4	5 6 7 8 9 10 11 12 1	13 14 15 16 17 18 19 20 21 22 23 24
12777: Branch : ucvtf f1, f0	F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Ds 1 2 3 4	5 6 7 8 9 10 11 12 1	13 14 15 16 17 18 19 20 21 22 23 24
12778: :: fdiv f0, f0, f	f1 F DC Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Ds 1 2 3 4	5 6 7 8 9 10 11 12 1	13 14 15 16 17 18 19 20 21 22 23 24
12779: Condition :: fmov f1, #1065	5353216 F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Is 1 2 Cm 1	2 3 4 5 6 7 8 9 1	10 11 12 13 14 15 16 17 18 19 20 2:
12780: I: fcmpe f0, f1	F Dc Rn 1 2 3 4	4 5 6 7 8 9 10	11 12 Ds 1 2 3 4	5 6 7 8 9 10 11 12 1	13 14 15 16 17 18 19 20 21 22 23 24
12781. 3102712 (CO. 13330). 0700400074: D.pl 0x400e88	F Dc Rn 1 2 3	3 4 5 6 7 8 9	10 11 Ds 1 2 3 4	5 6 7 8 9 10 11 12 1	13 14 15 16 17 18 19 20 21 22 23 24
12782: s182713 (t0: r3359): 0x00400e78: adrp x0, #5488	864 F Dc Rn 1 2 3	3 4 5 6 7 8 9	10 11 12 Is		
12783: s182714 (t0: r3360): 0x00400e7c: ldr x0, [x0, #	#3992] F Dc Rn 1 2 3		10 11 12 Ds Is		
12784: s182715 (t0: r3361): 0x00400e80: ldrb w0, [w0,	w1, SXTW] F 1 2 3 4	4 5 6 7 8 9 10	11 12 Dc Rn 1 Ds 1		
12785: s182716 (t0: r3362): 0x00400e84: bl 0x400bdc	F 1 2 3 4	4 5 6 7 8 9 10	11 12 Dc Rn 1 Is		
12786: s182717 (t0: r3363): 0x00400bdc: adrp x1, #5576	056 F 1 2 3		10 11 Dc Rn 1 Is		
12787: s182718 (t0: r3364): 0x00400be0: and x0, x0, #2	255 F 1 2 3		10 11 Dc Rn 1 Ds 1		
12788: s182719 (t0: r3365): 0x00400be4: ldr x2, [x1, #	#2656] F 1 2 3	3 4 5 6 7 8 9	10 11 Dc Rn 1 Ds Is		
12789: s182720 (t0: r3366): 0x00400be8: adrp x1, #5488	1864 F 1 2 3	3 4 5 6 7 8 9	10 11 Dc Rn 1 Is		
12790: s182721 (t0: r3367): 0x00400bec: ldr x1, [x1, #	#3968] F 1 2 3	3 4 5 6 7 8 9	10 11 Dc Rn 1 Ds Is		
127 <mark>91 · s182722 (to · r3368) · oxoo400bf</mark> 0: ldr x1, [x1]	F 1 2 3	3 4 5 6 7 8 9	10 11 Dc Rn 1 Ds 1		
127 127 127	x0, x2 F 1 2 3	3 4 5 6 7 8 9	10 11 12 Dc Rn 1 Ds		
127 Maicious IS b 0x400960	F 1 2 3	3 4 5 6 7 8 9	10 11 12 Dc Rn 1 Is		
127 50: sub sp, sp, #1	16 F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc Rn	1 Is	
	F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc Rn	1 Ds 1 2 3 4 5 6	7 8 9 10 11 12 13 14 15 16 17 18
127 38: str x0, [sp, #	#12] F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc Rn	1	
	F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc Rn		
127 7: isb	F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc		
127 <del>55. 3102730 (co. 13370). 07004005</del> 74: add sp, sp, #1	16 F 1 2		9 10 11 12 13 Dc		
12800: s182731 (t0: r3377): 0x00400978: ret	F 1 2	2 3 4 5 6 7 8	9 10 11 12 13 Dc		
12801: s182732 (t0: r3378): 0x00400e88: ldp_uop x29, >	x30, [sp]		8 9 10 11 12 Dc		
12802: s182733 (t0: r3379): 0x00400e88: addxi_uop sp,	sp, #48		8 9 10 11 12 13 Dc		
12803: s182734 (t0: r3380): 0x00400e8c: ret	F 1		8 9 10 11 12 13 Dc		
12804: s182735 (t0: r3381): 0x00400698: subs x3, #4			7 8 9 10 11 12 Dc		
12805: s182736 (t0: r3382): 0x0040069c: b.ls 0x4006b0			7 8 9 10 11 12 Dc		
12806: s182737 (t0: r3383): 0x004006b0: orr x1, xzr, >	x24	F 1 2 3 4 5	6 7 8 9 10 11 Dc		

### Allows to understand how the attack works

Instructions



### **DEFEATED BY THE BRANCH PREDICTOR**

### Cycles (Time)

Instructions

176001: s345932 (t0: r45933): 0x0040095c:	ret	F DC Rn 1 IS Cm 1
176002-0245022 (+045024). 000400054:	dsb	
1766	ldr x1, [sp, #28]	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Is Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 32 4 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
1766	ldr x0, [sp, #40]	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Is Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 32 42 52 62 72 82 9 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
1766 Attacked Branch	scvtf f0, f1	F Dc Rn 1 2 3 4 5 6 7 8 9 10 11 12 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 32 42 52 62 72 82 93 03 1 32 33 34 35 36 37 38 39 40 41 42 Is 1 Cm 1
1766	ucvtf f1, f0	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 Is 1 Cm 1
1766 Condition	fdiv f0, f0, f1	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Ds 1 2 3 4 5 6 7 8 9 10 11 12 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 Is 1 2 3 4 5 6 7 8 9 10 11 Cm 1
1766 ::	fmov f1, #1065353216	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Is 1 2 Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56
1766 ):	fcmpe f0, f1	F DC Rn 1 2 3 4 5 6 7 8 9 10 11 12 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 Is 1 Cm 1
176610. 5345941 (LO. 145942). 0X004000/4:	b.pl 0x400e88	F Dc Rn 1 2 3 4 5 6 7 8 9 10 11 Ds 1 2 3 4 5 6 7 8 9 10 11 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 Is Cm 1
1766	ldp_uop x29, x30, [sp]	F 1 2 3 4 5 6 7 8 9 10 11 DC Rn 1 IS Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
<sup>1766</sup> Malicious Part of	addxi_uop sp, sp, #48	F 1 2 3 4 5 6 7 8 9 10 11 DC Rn 1 IS Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
1760 Wallelous I alt 01	ret	F 1 2 3 4 5 6 7 8 9 10 11 Dc Rn 1 Ds 1 Is Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57
<sup>1766</sup> the Branch <b>Not</b>	subs x3, #4	F 1 2 3 4 5 6 7 8 9 10 Dc Rn 1 Is Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
1766 the Branon <b>Not</b>	b.ls 0x4006b0	F 1 2 3 4 5 6 7 8 9 10 Dc Rn 1 Ds Is Cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58
Taken	dsb	F 1 2 3 4 5 6 7 8 9 10 Dc Rn 1 Ds 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 Is Cm 1
1766	orr w1, wzr, w3	F 1 2 3 4 5 6 7 8 9 10 Dc Rn 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 15 Cm 1
1766	orr x0, xzr, x23	F 1 2 3 4 5 6 7 8 9 10 Dc Rn 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 18 0m 1
176019: s345950 (t0: r45951): 0x004006ac:	bl 0x400bfc	F 1 2 3 4 5 6 7 8 9 10 11 Dc Rn 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 Is cm 1
176020: s345951 (t0: r45952): 0x00400bfc:	addxi_uop ureg0, sp, #-96	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Is Cm 1
176021: s345952 (t0: r45953): 0x00400bfc:	strxi_uop x29, [ureg0]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 43 53 637 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Ds Is Cm 1
1/6022: s345953 (t0: r45954): 0x00400bfc:	strxi_uop x30, [ureg0, #8]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 44 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Ds Is Can 1
1/6023: s345954 (t0: r45955): 0x00400bfc:	addx1_uop sp, ureg0, #0	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 43 53 6 37 38 39 40 41 42 43 44 45 46 47 48 49 56 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Ds IS Ca 1
176024: \$345955 (t0: r45956): 0x00400c00:	add x29, sp, #0	F 1 Z 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 Z1 ZZ 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 49 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 DC RN 1 DS 1 15 Cm 1
176025: \$345956 (te: r45957): 0x00400c04:	addx1_dop urege, sp, #32	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 10 17 18 19 20 21 22 23 24 25 20 27 28 29 30 51 52 53 50 57 58 59 00 51 52 53 54 55 56 57 58 59 00 51 62 63 64 55 66 7 68 69 70 71 72 73 74 75 76 77 78 98 UC RN 1 US 1 15 Cm 1
176027: c245059 (t0: r45958); 0x00400c04:	strvi uon x22 [urego #2]	
176028: s345950 (t0: r45959); 0x00400c04;	adrn x22 #548864	
176020: 5345960 (to: r45960); 0x00400008;	shfm x21 x1 #0 #31	
176030: s345961 (t0: r45962): 0x00400c0c	addxi uop ureg0, sp. #48	
176031: s345962 (t0: r45963): 0x00400c10:	strxi_uop x23, [ureg0]	
176032: s345963 (t0: r45964): 0x00400c10:	strxi_uop x24, [ureg0, #8]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 44 55 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 58 69 70 71 72 73 74 75 76 77 78 79 80 80 10 81 10 8
176033: s345964 (t0: r45965): 0x00400c14:	adrp x24, #548864	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 2
176034: s345965 (t0: r45966): 0x00400c18:	adrp x23, #557056	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 43 53 637 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Ds Is Cm 1 2
176035: s345966 (t0: r45967): 0x00400c1c:	ldr x22, [x22, #3968]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 Dc Rn 1 Ds 1 Is Cm 1 2
176036: s345967 (t0: r45968): 0x00400c20:		F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 Dc Rn 1 Ds Is Cm 1 2
176037: s345968 (t0: r45969): 0x00400c24:	ldr x24, [x24, #3896]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 0c Rn 1 0s 1s 0m 1 2 3
176038: s345969 (t0: r45970): 0x00400c28:	addxi_uop ureg0, sp, #16	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 Dc Rn 1 18 Cm 1 2 3 4
176039: s345970 (t0: r45971): 0x00400c28:	strxi_uop x19, [ureg0]	F 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 Dc Rn 1 Ds 15 Cm 1 2 3

### Allows to visualize the root cause of a failed attack!

### **TRAINING SCENARIO**

## Instructions

Cycles (Time)



### We can even identify more scenarios...

	32	33	34 3	53	6 37	38	39	40	41	42	43																																	
31	32	33	34 3	5 3	6 37	38	39	40	41	42	43	44																																
32	33	34	35 3	6 3	7 38	39	40	41	42	Is	1	Cm	1																															
32	33	34	35 3	6 3	7 38	39	40	41	42	43	Is	1	Cm	1																														
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## FAITHFULNESS OF THE SIMULATION Comparing a real system and a simulation

Comparing a real system and a simulation

⇒ Very similar result of number of mispredicted branches

⇒ Helped to implement the attack on a real system

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Limitations

Comparing a real system and a simulation

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⇒ Helped to implement the attack on a real system

Limitations

⇒ **Slow** simulation, possibly **inaccurate** models

## CONCLUSION



## PAPER

### **Reproducing Spectre Attack with gem5**

How To Do It Right?

Pierre Ayoub pierre.ayoub@eurecom.fr EURECOM Sophia Antipolis, France

Pierre Ayoub and Clémentine Maurice. *Reproducing Spectre Attack with gem5: How To Do It Right?* (EuroSec '21), April 26, 2021

- GitHub: https://pierreay.github.io/reproduce-spectre-gem5/
- Contact: pierre.ayoub@eurecom.fr

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